

IDS 7/25/03 1/2

U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				ATTY. DOCKET NO. MI22-2348	SERIAL NO. Unknown 10/627468		
				APPLICANT Tyler A. Lowrey et al.			
				FILING DATE Filed herewith 7/25/03	GROUP Unknown 2812		
*Examiner Initial		Document Number	Date	U.S. PATENT DOCUMENTS			
JK	AA	6,159,818	12/00	Durcan et al.			
JK	AB	5,953,608	09/99	Hirota			
QW	AC	6,103,568	08/00	Fujiwara			
FOREIGN PATENT DOCUMENTS							
		Document Number	Date	Country	Class	Subclass	Translation
JK	AD	DE 199 07 062 A 1	11/99	Germany			Yes
JK	AE	EP 0 901 159 A2	10/99	EPO			No
OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)							
JK	AF	M. Asakura et al.; "A 34ns 256Mb DRAM with Boosted Sense-Ground Scheme"; IEEE International Solid-State Circuits Conference, 1994; 2 pages					
JK	AG	T. Inaba et al.; "A 250mV Bit-Line Swing Scheme for a 1V 4Gb DRAM"; 1995 Symposium on VLSI Circuits Digest of Technical Papers; pp. 99-100					
JK	AH	Takeshi Hamamoto et al.; "Cell-Plate-Line and Bit-Line Complementarity Sensed (CBCS) Architecture for Ultra Low-Power Non-Destructive DRAMs"; 1995 Symposium on VLSI Circuits Digest of Technical Papers; pp. 79-80					
JK	AI	Mikio Asakura et al.; "Cell-Plate Line Connecting Complementary Bitline (C') Architecture for Battery Operating DRAMS"; LSI Research and Development Laboratory; undated; pp. 59-60					
JK	AJ	Mikio Asakura et al.; "Cell-Plate Line Connecting Complementary Bit-Line (C') Architecture for Battery-Operating DRAM's"; IEEE Journal of Solid-State Circuits, Vol. 27, No. 4, April 1992; pp. 597-602					
JK	AK	Satoshi Shinozaki; "DRAMs in the 21st Century"; 1996 IEDM Short Course; 5 pages					
JK	AL	Nicky Chau-Chun Lu et al.; "Hal-V _{DD} Bit-Line Sensing Scheme in CMOS Dram's"; IEEE Solid-State Circuits, Vol. SC-19, No. 4, August 1994; pp. 451-454					
	AM						
EXAMINER	<i>Jennifer M. Kennedy</i>			DATE CONSIDERED	November 24, 2004		
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.							

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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2348	SERIAL NO. 101627, 468		
LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)				APPLICANT Tyler A.. Lowrey et al.			
		FILING DATE 7/25/03	GROUP 2812				
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*Examiner Initial		Document Number	Date	Name	Class Subclass Filing Date If Appropriate		
gk	AA	5,759,893	06/98	Wu			
gk	AB	6,184,081 B1	02/01	Jeng et al.			
gk	AC	6,037,234	03/00	Hong et al.			
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gk	AE	5,770,500	06/98	Batra et al.			
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		Document Number	Date	Country	Class	Subclass	Translation
gk	AL	DE 195 43 539 C 1	04/97	Germany			Yes No
gk	AM	WO 96/28844	09/96	PCT			
gk	AN	JP 411274434 A	10/1999	Japan (Sako)			
	AO						
	AP						
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	AR						
	AS						
	AT						
EXAMINER	Gunnar M. Kennedy		DATE CONSIDERED November 24, 2004				
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LIST OF ART CITED BY APPLICANT <small>(use several sheets if necessary)</small>				APPLICANT Tyler A. Lowsey et al.				
				FILING DATE July 25, 2003	GROUP 2811 2812			
*Examiner Initial		Document Number	Date	U.S. PATENT DOCUMENTS				
JG	AA	6,300,652 B1	10/9/2001	Risch et al.				
JG	AB	6,013,549	1/11/2000	Han et al.				
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JG	AD	6,165,840	12/26/2000	Choi et al.				
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	AE						Yes	No
	AF							
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	AG							
	AH							
	AI							
	AJ							
	AK							
	AL							
EXAMINER <i>Jeff M. Kennedy</i>			DATE CONSIDERED <i>November 24, 2004</i>					
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